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10/606,693	06/26/2003	Hoon Jang	20063/10001	5344

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EXAMINER

KEBEDE, BROOK

ART UNIT PAPER NUMBER

2823

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

10/606,693

**Applicant(s)**

JANG ET AL.

**Examiner**

Brook Kebede

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 June 2003.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-6 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 9/22/03.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Drawings***

2. Figures 1a, 1b, 1c, and 2a should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "forming CMOS image sensor on an epitaxial wafer," as recited in claim 1, line 3, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must

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be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

#### *Claim Objections*

4. Claim 1 is objected to because of the following informalities:

Although an attempt has been made to identify all instances of claim language non-compliance, such identification is extremely burdensome due to the large number of instances. Examples are provided herein below. Since such noncompliance confuses the claims to the extent that not all of the problems are readily apparent, then upon amendment, if an alternative interpretation of claim language requires a change in the rejection, the new rejection may properly be made final.

Claim 1 recites the limitation "forming a first photoresist layer over said structure, **patterning** so as to form a shallow trench on a pixel area, **and, etching**" in lines 6-7. However, it is not clear what "etching" does. Does it mean etching the first resist layer? Does it mean that etching the to form the shallow trench? In addition, it is not clear what layer is being patterned. Appropriate correction is required.

Applicants' cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' admitted prior art (Figs. 1a-2a) in view of Yaung et al. (US/6,372,603).

Re claim 1, Applicants' admitted prior art disclose a method for making complimentary metal oxide semiconductor (CMOS) image sensor, comprising: forming a CMOS image sensor on an epitaxial wafer (see Fig. 1a Applicants' admitted prior art **background** in Page 2, Paragraph [0006]), having a structure including an epitaxial layer (2) doped with a low concentration positioned on a p-type or n-type substrate (1) doped with a high concentration; forming a first photoresist layer (4) over said structure (see Fig. 1b); forming shallow trench isolation (3) prior forming the first resist layer, removing said first photoresist layer (4) (see Applicants' admitted prior art Figs. 1a-2a).

However, Applicants' admitted prior art does not specifically disclose forming a second photoresist layer over said structure, patterning so as to form a photodiode junction, and, then, conducting ion-implanting process; and removing said second photoresist layer and conducting a thermal treatment process.

Yaung et al. disclose a method of forming CMOS image sensor device the method includes forming the resist layer to pattern a mask layer (240) that formed over the substrate (see Fig. 2A); patterning the substrate to form shallow trench structure that going to be used to form photodiode junction (280) (see Fig. 2C); forming the second photoresist layer (270) and patterning the second photoresist layer and implanting the substrate to form photodiode junction (280); removing the second photoresist layer and annealing the substrate to uniformly diffuse the implanted ions in order to meet the specification and requirements of CMOS image sensor product (see Yaung et al. Figs. 2A-2E; Col. 2, line 65 – Col. 4 line 14).

Both Applicants' admitted prior art and Yaung et al. teachings are directed to fabricating CMOS image sensor photodiode devices. Therefore, the teachings of Applicants' admitted prior art and Yaung et al. are analogous.

Hence, one of ordinary skill in the art would have been motivated to look to analogous art teachings to form photoresist layer over the substrate, and forming trench by patterning the substrate to conduct ion-implanting process and conducting a thermal treatment process to form photodiode junction after the resist layer removed in order to fabricate high performance photodiode that possessed low leakage junction (see Yaung et al. Col. 1, line 55 – Col. 2, line 38).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Applicants' admitted prior art with to

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form photoresist layer over the substrate, forming trench by etching the substrate, conducting ion-implanting process and removing the photoresist layer and then conducting a thermal treatment process to form photodiode junction as taught by Yaung et al. in order to fabricate high performance photodiode that possessed low leakage junction.

Re claim 2, as applied to claim 1 above, Applicants' admitted prior art and Yaung et al. in combination disclose all the claimed limitations including the limitation wherein said first and second photoresist layers.

With regard to the limitation of ashing process to remove the resist layer Examiner takes an Official notice because it is well-known in the art to use a process such as plasma oxygen ashing in order effectively to remove the resist layer after completion of the resist masking task. See *In re Malcolm*, 129 F.2d 529, 54 USPQ 235 (CCPA 1942). See *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420 (CCPA 1970).

Re claim 3, as applied to claim 1 above, Applicants' admitted prior art and Yaung et al. in combination disclose all the claimed limitations including the limitation wherein said thermal treatment is performed by rapid thermal annealing (RTA) or furnace annealing at predetermined temperature. Furthermore, the claimed temperature range would have been achieved within the level of ordinary skill in the art.

Therefore, it would have been to one having ordinary skill in the art at the time of the invention is made to set the claimed furnace anneal temperature, since it has been held where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955); *In re Hoeschele*, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969); *Merck & Co. Inc. v. Biocraft Laboratories Inc.*, 874 F.2d 804, 10 USPQ2d 1843 (Fed.

Cir.), cert. denied, 493 U.S. 975 (1989); *In re Kulling*, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and *In re Geisler*, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997). Furthermore, the specification contains no disclosure of either the critical nature of the claimed anneal temperature or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 4, as applied to claim 1 above, Applicants' admitted prior art and Yaung et al. in combination disclose all the claimed limitations including the limitation wherein a final profile doped in said epitaxial layer doped with a low concentration is formed on the top of a shallow trench isolation layer (see Applicants' admitted prior art Figs. 1a-2a and Yaung et al. Figs. 2A-2E; Col. 2, line 65 – Col. 4 line 14).

Re claim 5, as applied to claim 1 above, Applicants' admitted prior art and Yaung et al. in combination disclose all the claimed limitations including the limitation forming the shallow trench at predetermined depth. Furthermore, the claimed depth range would have been within the scope of Applicants' admitted prior art and Yaung et al. disclosure and achieved within the level of ordinary skill in the art by routine optimization.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that



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the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed trench depth or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d, 1936 (Fed. Cir. 1990).

Re claim 6, as applied to claim 1 above, Applicants' admitted prior art and Yaung et al. in combination disclose all the claimed limitations including the limitation wherein the shallow trench is filled with a dielectric selected from the group consisting of oxide, nitride, oxinitride, and silicate glass by spin coating, chemical vapor deposition (CVD), or diffusion methods (see Applicants' admitted prior art Figs. 1a-2a and Yaung et al. Figs. 2A-2E; Col. 2, line 65 – Col. 4 line 14).

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Nishizawa et al. (US/4,536,946) and Pan et al. (US/6,329,233) also disclose similar inventive subject matter.

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*Correspondence*

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede  
Examiner  
Art Unit 2823



BK  
September 29, 2004